



**PROCEEDINGS OF
THE FIRST INTERNATIONAL CONFERENCE
ON
SCIENCE AND ENGINEERING**

Volume - 1

**Electronics
Electrical Power
Information Technology
Engineering Physics**

**Sedona Hotel, Yangon, Myanmar
December 4-5, 2009**

**PROCEEDINGS OF THE
FIRST INTERNATIONAL CONFERENCE
ON
SCIENCE AND ENGINEERING**

Volume - 1

**Electronics
Electrical Power
Information Technology
Engineering Physics**

**Organized by
Ministry of Science and Technology**

**DECEMBER 4-5, 2009
SEDONA HOTEL, YANGON, MYANMAR**

ELECTRICAL POWER ENGINEERING

Designing and Modeling of Dynamic Voltage Restorers for Power Quality Control in Myanmar Info-Tech

Zar Zar Tun

Department of Electrical Power Engineering, Yangon Technological University
Yangon, Myanmar
dzztun@gmail.com

Abstract— Voltage sags and swells in the medium and low voltage distribution grid are considered the most frequent type of power quality problems based on recent power quality studies. Their impact on sensitive loads is severe. Different solutions have been developed to protect sensitive loads against such disturbances. Among them, DVR is considered to be the most efficient and effective solution. Its appeal includes lower cost, smaller size and its dynamic response to the disturbance. This paper described DVR principles and voltage restoration methods for balanced and/or unbalanced voltage sags and swells in a distribution system. DVR is a powerful custom power device used for short duration voltage compensation of sensitive loads against voltage disturbances in power distribution lines. The presentation will focus on the technical market requirements and the proposed solution for Myanmar Info-Tech, which is the largest computer and software industry in Myanmar. Myanmar Info-Tech is often encountering power quality problem including voltage sag/swell and short interruption. To overcome these problems, the DVR solution is introduced in this paper with Matlab simulation.

Keywords— Dynamic Voltage Restorer (DVR), voltage sags/swells, power quality, MOSFET VSI

I. INTRODUCTION

One of the major concerns in electricity industry today is power quality problems to sensitive loads. This is due to the advent of a large numbers of sophisticated electrical and electronic equipment. The use of these equipments very often requires power supplies with very high quality. Voltage sag, which is a momentary decrease in rms voltage magnitude in the range of 0.1 to 0.9 per unit (p.u.), is considered as the most serious problem of power quality [1]. It is often caused by faults in power systems or by starting of large induction motors. It can interrupt or lead to malfunction of any electric equipment, which is sensitive to voltage variations. It occurs more frequently than any other power quality phenomenon does.

During power disturbances DVR installed in front of a critical load will appropriately provide correction to that load only. It is noteworthy that during normal operation due to the series connection a DVR may have to provide a small amount of voltage drop mainly at the coupling transformer. Also DVR cannot provide compensation during full power interruptions. In this paper modeling and simulation of DVR for protection against voltage sag/swell for Myanmar Info-Tech is

described. Then, a design modeling and simulation of the DVR is presented.

II. DYNAMIC VOLTAGE RESTORERS

The main components of DVR are energy storage unit, voltage source inverter circuit and filter unit and series injection transformers as shown in Fig.1. DVR is used for the protection of sensitive loads from voltage sags/swells coming from the network. The sags/swells voltages are occurred for short time intervals (transient condition). The voltage sags are due to the fault conditions and the swells are caused by the drop-out of the large load from the system. Thus the DVR is located at the incoming sides of sensitive load as shown in Fig. 1. If a fault occurs on nearby lines, DVR insert a series voltage V_{DVR} and compensate the load voltage to pre-fault value. In the same way, if a large load is shut-down, the DVR insert the negative DVR voltages which are 180° phase shift from the supply voltage. Thus the load voltage will be constant at the nominal value under transient condition. This means that any differential voltage caused by transient disturbances in the AC feeder will be compensated by an equivalent voltage generated by the DVR.

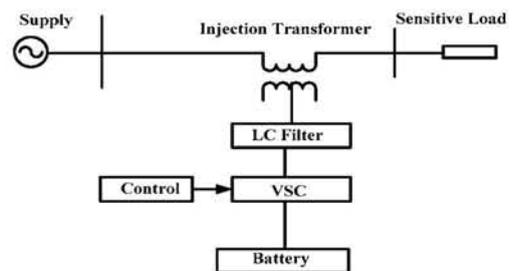


Fig. 1 Schematic diagram of DVR system

DVR has two modes of operation as standby mode and boost mode. In standby mode, the injection transformer primary winding is shorted causing no switching of the semiconductor switches and reduced the losses. The DVR will be operated most of the time in this mode. In boost mode, the DVR is injecting compensation voltage through the injection transformer due to the detection of a supply voltage disturbance. An equivalent circuit diagram of

the DVR and the principle of series injection for sag compensation are depicted in Fig. 2.

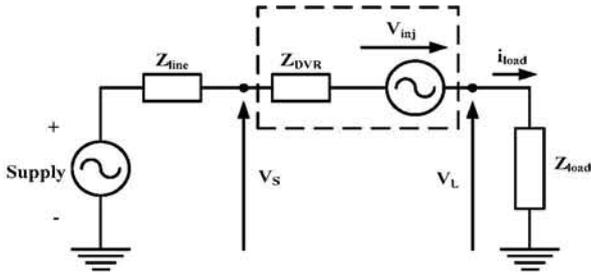


Fig. 2 Equivalent circuit of DVR

As the mathematical expression:

$$V_L(t) = V_s(t) + V_{inj}(t) \quad (1)$$

where $v_L(t)$ is the load voltage, $v_s(t)$ is the sagged supply voltage and $v_{inj}(t)$ is the voltage injected by the mitigation device as shown in Fig. 2. Under nominal voltage conditions, the load power on each phase is given by (2):

$$S_L = V_L I_L^* = P_L - jQ_L \quad (2)$$

where I_L is the load current, and P_L and Q_L are the active and reactive power taken by the load, respectively, during a sag/swell. When the mitigation device is active and restores the voltages back to normal, the following applies to each phase:

$$S_L = P_L - jQ_L = (P_s - jQS_s) + (P_{inj} - jQ_{inj}) \quad (3)$$

where the sag subscript refers to the sagged supply quantities. The inject subscript refers to quantities injected by the mitigation device [2].

III. PRINCIPLE OF THE DVR OPERATION

The DVR is connected in series with power distribution line as shown in Fig. 1. The DVR is able to control the voltage across a sensitive load by injecting an appropriate voltage phasor through an injection transformer. As a result, any voltage disturbance appears in up-stream can be compensated through the DVR and the disturbance is unseen to the load.

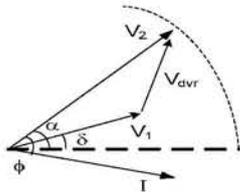


Fig.3 Phasor diagram of power distribution system during sag

In Fig. 3, V_1 , V_2 , V_{dvr} are the post-sag supply voltage magnitude, compensated load voltage magnitude and the DVR injected voltage magnitude respectively. Moreover I , p , f , δ , α represent load current, load power factor angle, supply voltage phase angle deviation and load voltage advance angle respectively. If P_{in} and P_{out} are the input powers from the source and load power respectively, then the DVR supply can be obtained as follow;

$$P_{out} = P_{dvr} + P_{in} \quad (4)$$

where P_{dvr} is the DVR supplied power during the sag/swell condition. It has been shown that the supply of energy by the DVR for voltage restoration can be kept minimum, by advancing all three phases with a certain advance angle α . This control method is usually known as α -control. The magnitude of the DVR injection voltage and the real power supplied by the DVR can be calculated from Fig. 4 by using cosine rule as:

$$V_{dvr}^2 = V_2^2 + V_{1j}^2 - 2 V_2 V_{1j} \cos(\alpha - \delta_j) \quad (5)$$

where j represents for phases a, b and c. Then the power rating of DVR with the three phase balanced fault is;

$$P_{dvr} = 3 V_{dvr} I \cos \theta \quad (6)$$

Also, the energy needs to be stored in the DVR storage unit can be formulated as:

$$E_{dvr} = P_{dvr} \times T_{sag} \quad (7)$$

where T_{sag} is the maximum sag/swell duration in second. The necessary condition for correcting a sag/swell without supplying energy from DVR will be obtained when θ is 90° .

IV. MODELING OF DVR

The compensation of voltage sag/swell can be limited by a number of factors, including finite DVR power rating, loading conditions, power quality problems and types of sag/swell. DVR is able to handle most sags/swells and the performance must be maximized according to the equipment inserted. Otherwise, the DVR may not be able to avoid tripping and even cause additional disturbance to the loads.

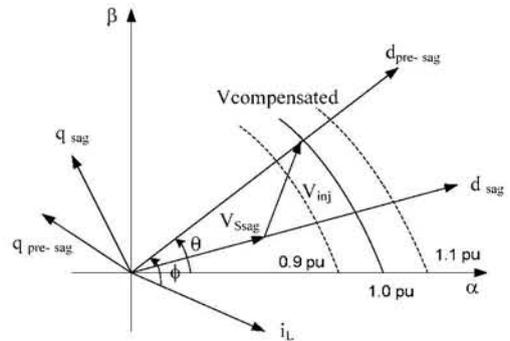


Fig. 4 Compensation strategy of DVR for voltage sag

The control strategy should be able to compensate for any of voltage sag/swell and consider the limitation the DVR. Fig. 4 shows the supply voltage vector during the pre-sag stage which is represented as $V_{S \text{ pre-set}}(t)$ on the $d_{\text{pre-set}}$ axis in which the rotating phase angled is derived from Phase Lock Loop (PLL) [3]. Initially, the load voltage vector $V_L(t)$ is the same as $V_{S \text{ pre-set}}(t)$ and is assumed to be 1.0 p.u. if the voltage drops across the series transformer are neglected. When the voltage sags occur, the actual source voltage vector $V_S(t)$ is moved to $V_{S \text{ sag}}(t)$. To restore the load voltage vector $V_L(t)$, an injected voltage vector $V_{inj}(t)$ is provided by the DVR. A similar compensation strategy can be drawn in the form of a phasor diagram for voltage swell as well.

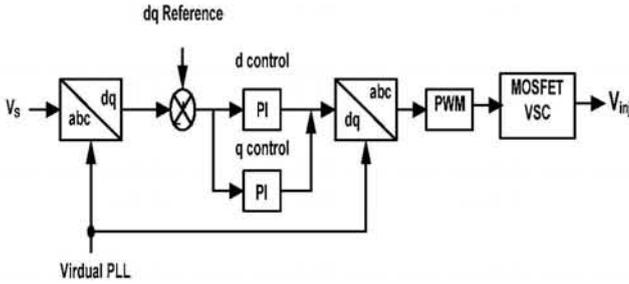


Fig. 5 Control structure of DVR

Fig. 5 shows the basic control scheme and parameters that are measured for control purposes. When the grid voltage is at its normal level the DVR is controlled to reduce the losses in the DVR to a minimum. When voltage sags/swells are detected, the DVR should react as fast as possible and inject an AC voltage to the grid. It can be implemented using a feedback control technique based on the voltage reference and instantaneous values of supply and load voltage. The control algorithm produces a three phase reference voltage to the series converter that tries to maintain the load voltage at its reference value. The voltage sag is detected by measuring the error between the d-q voltage of the supply and the reference values [4]. The d-reference component is set to a rated voltage and the q-reference component is set to zero. The abc to dq0 transformation is carried out as:

$$V_d = \frac{2}{3} [V_a \sin \omega t + V_b \sin(\omega t - \frac{2\pi}{3}) + V_c \sin(\omega t + \frac{2\pi}{3})]$$

$$V_q = \frac{2}{3} [V_a \cos \omega t + V_b \cos(\omega t - \frac{2\pi}{3}) + V_c \cos(\omega t + \frac{2\pi}{3})]$$

$$V_0 = \frac{1}{3} [V_a + V_b + V_c] \quad (8)$$

The dq0 to abc transformation is carried out as:

$$V_a = [V_d \sin \omega t + V_q \cos \omega t + V_0]$$

$$V_b = [V_d \sin(\omega t - \frac{2\pi}{3}) + V_q \cos(\omega t - \frac{2\pi}{3}) + V_0]$$

$$V_c = [V_d \sin(\omega t + \frac{2\pi}{3}) + V_q \cos(\omega t + \frac{2\pi}{3}) + V_0] \quad (9)$$

The supply voltage is connected to a transformation block that converts stationary frame to dq-frame In Fig.5. Virtual PLL is also applied so that the input abc voltage is converted to corresponding dq values. This virtual is internally generated from the simulink. These dq values are compared with reference dq voltages and the differences are detected by the error detector. Then the error voltages are conditioned by PI controllers to catch the nominal values. The resultant voltages are applied to PWM which control MOSFET VSI so that the constant abc voltage is applied to the load.

V. SYSTEM STUDY AT MYANMAR INFO-TECH

This paper is intended to carry out the design, modeling and simulation of DVR for Myanmar Info-Tech. It is currently the largest computer and software industry in Myanmar. The current power supply one line diagram of Myanmar Info-Tech is as shown below.

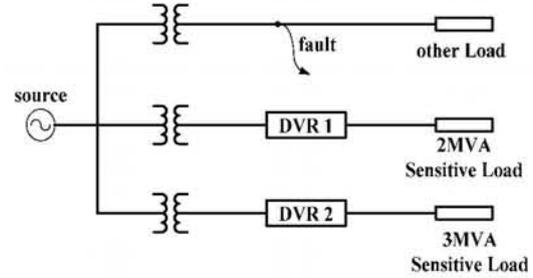


Fig.6 The Single line diagram of Myanmar Info-Tech

The total load of Myanmar Info-Tech is focused to be 5 MVA in future. Currently utilization of the total load is about 1 MVA at normal operation condition and at peak load it is about 1.25 MVA. The propose DVR model is considered for the long term load i.e 5MVA which will be supplied by 2MVA portion and 3MVA portion according to the existing scheme as shown in Fig. 6.

The DVR is connected in series with power distribution line. The DVR is able to control the voltage across a sensitive load of InfoTech by injecting an appropriate voltage through the injection transformers. Consequently, any voltage disturbance appears in up-stream can be compensated by the DVR and the disturbance is unnoticed to the load. The simulated design data is shown in Table 1 and simulink block diagram is expressed in Fig. 7.

In order to show the performance of the DVR in voltage sags and swells mitigation, a Myanmar Info-Tech distribution network is simulated using Matlab. The DVR are connected to the system through series transformers with a capability to insert a maximum voltage of 50 % of the phase to ground system nominal voltage. The load considered in the study is a 5.0 MVA (2 MVA and 3 MVA) capacity with 0.8 p.f,

lagging. The three phase fault at the nearby load line is considered with Matlab/Simulink simulation.

TABLE I
DESIGN PARAMETERS FOR TWO DVRs OF MYANMAR INFO-TECH

| Sr. No | Appliance | Design Parameter |
|--------|---|--|
| 1 | <u>Three Phase Fault</u> | $R = 0.00001\Omega$ $t = 0.2 \sim 0.4$ s $R_p = 1 M\Omega, C_p = \text{inf}$ |
| 2 | <u>2 MVA DVR</u> a. Load b. Three Phase Injection Transformer c. LC Filter d. PI Controller | $V_n = 400$ V, $f_n = 50$ Hz $P = 1.6$ MW, $Q_L = 1.2$ MVAR $S = 2$ MVA Winding 1 Parameters, $V_1 = 1.6$ kV $R_1 = 0.002$ pu, $L_1 = 0.05$ pu Winding 2 Parameters, $V_2 = 400$ V $R_2 = 0.0002$ pu, $L_2 = 0.005$ pu Core Parameters, $R_m = 20$ pu, $L_m = 20$ pu $L = 3$ mH, $Q_C = 150$ kvar $K_p = 20, K_i = 0.01$ |
| 3 | <u>3 MVA DVR</u> a. Load b. Three Phase Injection Transformer c. LC Filter d. PI Controller | $V_n = 400$ V, $f_n = 50$ Hz $P = 2.4$ MW, $Q_L = 1.8$ MVAR $S = 2$ MVA Winding 1 Parameters, $V_1 = 2.0$ kV $R_1 = 0.002$ pu, $L_1 = 0.05$ pu Winding 2 Parameters, $V_2 = 400$ V $R_2 = 0.00002$ pu, $L_2 = 0.0005$ pu Core Parameters, $R_m = 20$ pu, $L_m = 20$ pu $L = 3$ mH, $Q_C = 180$ kvar $K_p = 20, K_i = 0.01$ |

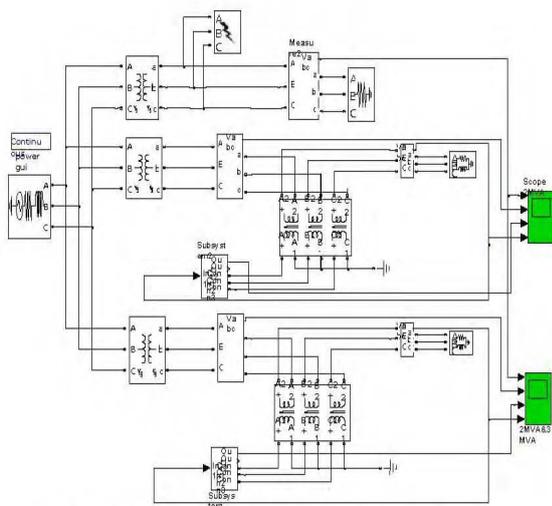


Fig. 7 Simulink block diagram for two DVRs

VI. THE SIMULATION RESULTS

A. Impact on Voltage Sags

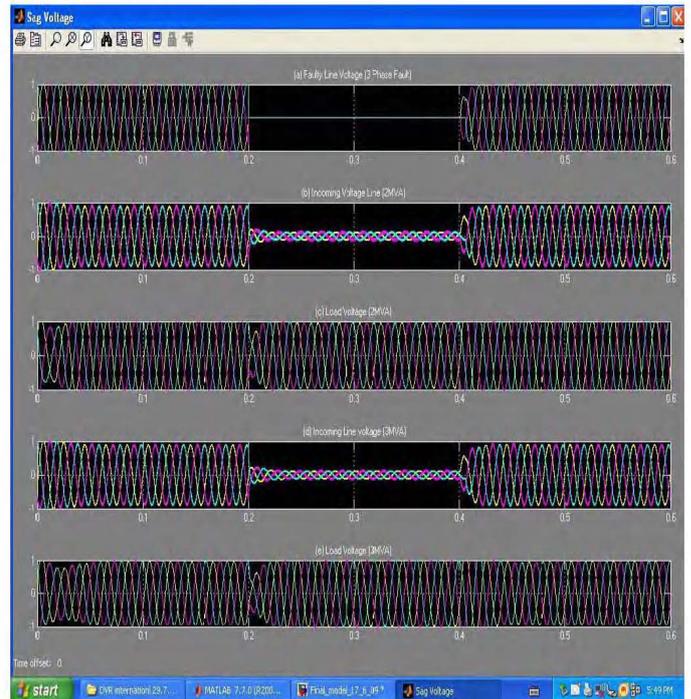


Fig. 8. Three-phase voltage sag at 2MVA and 3MVA load; (a) Faulty line voltage, (b) Incoming line voltage (2MVA), (c) Load voltage (2MVA) (d) Incoming line voltage (3MVA), (e) Load voltage (3MVA)

A case of Three-phase voltage sag is simulated and the results are shown in Fig. 6. Fig. 8 (a) shows a 50% voltage sag initiated at 200 ms and it is kept until 400 ms, with total voltage sag duration of 200 ms. Fig. 8 (b) show the voltage injected by the DVR at 2MVA and Fig. 8 (d) show the voltage injected by the DVR at 3MVA and the compensated load voltages are shown at 8 (c) and 8 (e). As a result of DVR, the load voltage is kept at 1 p.u. throughout the simulation, including the voltage sag period. DVR quickly injects necessary voltage components to smooth the load voltage upon detecting voltage sag. As can be seen from the results, the DVR was able to produce the required voltage component rapidly and helped to maintain a balanced and constant load voltage at 1.00 p.u.

B. Impact on Voltage Swells

The performance of DVR for a voltage swell condition is investigated. Here, the supply voltage swell is generated and the DVR injected voltage and load voltages at 2 MVA and 3 MVA loads are shown in Fig. 9. The supply three-phase voltage amplitudes were increased about 150% of nominal voltage. The injected three-phase voltage that is produced by DVR in order to correct the load voltages is also shown. As can be seen from the results, the load voltage was kept at the nominal value with the help of the DVR. Similar to the case

of voltage sag, the DVR reacted quickly to inject the appropriate voltage component (negative voltage magnitude) to correct the supply voltage.

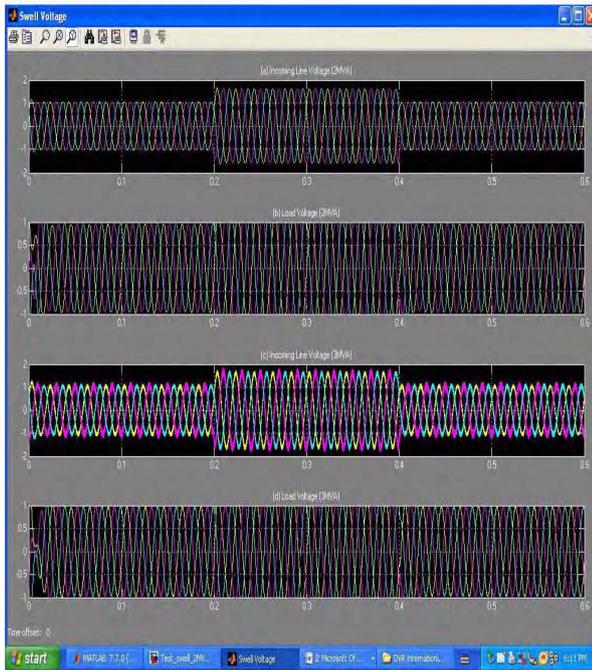


Fig. 9 Three-phase voltage swell at 2MVA; and 3MVA load:(a) Incoming line voltage (2MVA), (b) Load voltage (2MVA) (c) Incoming line voltage (3MVA), (d) Load voltage (3MVA)

VII. CONCLUSION

The aspects of voltage sag/swell mitigation have been studied. DVR with its modeling aspects has been studied and then also examined for its performance at the sensitive loads. DVR has excellent performance to protect sensitive loads. It can deal with all levels of sag severity- shadow, severe and worst. DVR is specially designed to mitigate the voltage sag up to 50% and the swell of 50 % of its nominal voltage. Performance of a DVR in mitigating voltage sags/swells is demonstrated with the help of Matlab. MOSFET VSI converter is considered in the DVR to inject the required voltage and LC filter is employed to smooth this voltage. The voltage sag/swell are causing the computers and related appliances such as scanners, printers, IT devices to fail or shutdown as well as create current unbalance that could blow fuses or trip breakers. These effects causes malfunction of operations, internet connection breakdown and equipment damage. Thus design and modeling of DVR is executed for Myanmar Info-Tech to avoid these power quality problems.

ACKNOWLEDGMENT

The author is deeply grateful to Daw Than Than Win, Professor and Head, Department of Electrical Power Engineering, Yangon Technological University, for her willingness to share her ideas and helpful suggestions. The

author also wishes to thank Dr.Aung Zeya, Lecturer, Department of Electrical Power Engineering, Yangon Technological University, for his encouragement, help, support and guidance. The author is extremely grateful thanks to Daw Naing Naing Maw, Lecturer, Department of Electrical Power Engineering, Yangon Technological University, for her skillful guidance and encouragement. The author greatly expresses her thanks to all persons whom will concern to support in preparing this paper.

REFERENCES

- [1] IEEE recommended practice for evaluating electric power system compatibility with electronic process equipment, IEEE Standard 1346-1998. 1998.
- [2] Paisan Boonchiam and Nadarajah Mithulananthan, "Understanding of Dynamic Voltage Restorers Through MATLAB Simulation", *Thammasat Int. J. Sc. Tech.*, Vol. 11, No. 3, July-September 2006
- [3] Ming Hu and Heng Chen, "Modeling and Controlling of Unified Power Quality Component", in *APSCOM-00*, 2, pp. 431- 435,2000.
- [4] Sybille and P. Giroux, "Simulation of FACTS Controllers Using the MATLAB Power System Blockset and Hypersim Real-Time Simulator", *IEEE Power Eng. Society*, 1, pp. 488-491, 2002.